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EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,950	THURSTON, ANDREW J.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/8/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Applicant's request for reconsideration filed on 11/8/2004 has been reviewed.

2. Amendment filed on 11/8/2004 has been entered.

3. Applicant's arguments filed on 11/8/2004 have been fully considered but they are not deemed to be persuasive.

4. The applicant contends, "the cited art fails to anticipate, teach, or suggest: "extracting an error polynomial from the data signal based on no more than six equations having no more than two branch decisions," as recited in claim 1.

The examiner disagrees and asserts that Shen et al. (U.S. 6,199,188 B1) teaches, " the syndrome generator sends the syndromes to an error locator polynomial generator 14, which produces in a conventional manner from the syndromes an error locator polynomial of degree, e, where e is the number of errors in the code word", (error locator polynomial generator 14 in figure 1, col. 4, lines 40-43, Shen et al.). As per claim 1, "based on no more than six equations having no more than two branch decisions", means the number of equations and the branch decisions can be zero. Hence the prior art Shen et al. teaches the limitations of claim 1.

5. The applicant contends, "With respect to claim 13, neither Shen nor Oh teaches using Galois field multiply accumulators to calculate a plurality of minimum-degree polynomials".

The examiner disagrees and asserts that Shen et al. teach that the mathematical operations of addition, subtraction, multiplication and division discussed herein are Galois field operations over the applicable Galois Fields (col. 4, lines 32-34, Shen et al.). Oh et al. teach that 4t multipliers in the Galois field are needed and each iteration is completed in 2 clock cycles (figure 1A to 1C, col. 5, lines 46-48, Shen et al.).

6. The applicant contends that with respect to claim 25, the cited art fails to teach or suggest, "using said Galois field multiply accumulators to generate an error polynomial based on values provided at said syndrome inputs, by executing no more than six equations with two branch decisions".

The examiner disagrees and asserts that as per claim 25, "by executing no more than six equations with two branch decisions" means zero equation can be executed to generate an error polynomial. Shen et al. teach that the mathematical operations of addition, subtraction, multiplication and division discussed

herein are Galois field operations over the applicable Galois Fields (col. 4, lines 32-34, Shen et al.). Shen et al. teach that using the error syndromes, the system determines an error locator polynomial, which is a polynomial that has the same degree as the number of errors (col. 1, lines 53-55, Shen et al.).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 5, 9, 10, 11, 12, 25, 30, 31, 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Shen et al. (US 6,199,188 B1). For detailed rejection, please refer to the office action mailed on 8/25/2004.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 2-4, 6, 13, 14, 18, 24, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) as applied to claim 1 above, and further in view of Oh et al. (US 5,583,499). For detailed rejection, please refer to the office action mailed on 8/25/2004.

12. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) as applied to claim 1 above, and further in view of Erhart et al. (US 5,051,999). For detailed rejection, please refer to the office action mailed on 8/25/2004.

13. Claims 8, 27, 28, 29, 33, 34, 35, 36, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) as applied to claim 1 and 25 above, and further in view of Stenerson (US 4,597,083). For detailed rejection, please refer to the office action mailed on 8/25/2004.

14. Claims 15-17, 19, 20, 21, 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) and Oh et al. (US 5,583,499) as applied to claim 13 above, and further in view of Stenerson (US 4,597,083). For detailed rejection, please refer to the office action mailed on 8/25/2004.

15. Claims 38, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (US 4,504,948) in view of Stenerson (US 4,597,083).

As per claim 38, Patel teaches a decoder circuit (figure 1, col. 4, lines 13-14, Patel) to generate an error polynomial based on the following six equations:

(1) $d_0 = S_1$,

(2) $d_1 = S_3 + S_1S_2$,

(3) $\sigma^1(X) = 1 + S_1X$,

(4) if ($d_1 = 0$) then $\sigma^2(X) = \sigma^1(X)$

else if ($d_0 = 0$) then $\sigma^2(X) = q_0\sigma^1(X) + d_1X^3$

else $\sigma^2(X) = q_0\sigma^1(X) + d_1X^2$,

(5) $d_2 = S_5\sigma 0 + S_4\sigma 1 + S_3\sigma 2 + S_2\sigma 3$, and

(6) if ($d_2 = 0$) then $\sigma^3(X) = \sigma^2(X)$

else $\sigma^3(X) = q_1\sigma^1(X) + d_1X^3$,

where S_i are the syndromes, σ^i are minimum-degree polynomials, σ_1 are four coefficients for $\sigma^2(X)$, d_0-d_2 are correction factors, q_0-q_1 are additional correction factors, q_0 is equal to d_0 unless d_0 is zero, when q_0 is 1, and q_1 is equal to d_1 unless d_1 is zero, when $q_1 = q_0$ (figure 1, col. 4, lines 27-45; col. 5, lines 29-58; col. 7, lines 34-62; col. 8, lines 43-47; col. 8, line 66 to col. 9, line 25; col. 10, lines 24-29, Patel). However Patel does not explicitly teach the specific use of a plurality of Galois field multiply accumulators; and a state machine programmed to use the Galois field multiply accumulators.

Stenerson in an analogous art teaches that the Galois field products from the multiplier 124 (in the form of a PROM programmed as shown in FIGS. 18C and 18D corresponding to multiplying by ff, the coefficient of the fourth term of the polynomial) are summed by exclusive-ORs 132 with the corresponding outputs of the latches 130, delayed one byte or term of the respective input data block, and their sums applied through shift registers 134 to latches 136. The multiplying circuits 124 and 126 operate like the multiplying circuit 114 of the syndrome generator 102 (figure 8, col. 18, lines 28-35, lines 52-53, Stenerson).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel's patent with the teachings of Stenerson by including an additional step of using a plurality of Galois field multiply accumulators; and a state machine programmed to use the Galois field multiply accumulators.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a plurality of Galois field multiply accumulators; and a state machine programmed to use the Galois field multiply accumulators would provide the opportunity to reduce the number of circuit elements and increase the processing speed of the decoder circuit for error correction.

- As per claim 40, Patel and Stenerson teach the additional limitations.

Stenerson teaches the decoder circuit wherein said state machine is programmed to operate a selected one or more of said Galois field multiply accumulators in a pass-through mode (col. 18, lines 28-33, col. 22, lines 30-34, Stenerson).

16. Claims 39, 46, 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (US 4,504,948) and Stenerson (US 4,597,083) as applied to claim 38 above, and further in view of Maki et al. (US 4,873,688).

As per claim 39, Patel and Stenerson substantially teach the claimed invention described in claim 38 (as rejected above).

However Patel and Stenerson do not explicitly teach the specific use of the decoder circuit wherein each of the Galois field multiply accumulators represents a different power of the error polynomial.

Maki et al. in an analogous art teach that the VLSI cells used throughout the decoder include the following Galois Field processing elements: adder, constant multiplier, general multiplier, and field inverse. The constant multiplier performs the operation...in the field defined in Table 1 (col. 5, lines 11-29, Maki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel's patent with the teachings of Maki et al. by including an additional step of using the decoder circuit wherein each of the Galois field multiply accumulators represents a different power of the error polynomial.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoder circuit wherein each of the Galois field multiply accumulators represents a different power of the error polynomial would provide the opportunity to reduce the number of circuit elements and increase the processing speed of the decoder circuit for error correction.

- As per claim 46, Patel, Stenerson and Maki et al. teach the additional limitations.

Maki et al. teach the decoder circuit wherein: at least one of said Galois field multiply accumulators has a first multiplexer whose output is coupled to a first input of a Galois field multiplier, a second multiplexer whose output is coupled to a second input of said Galois field multiplier, and a third multiplexer whose output is coupled to a first input of a Galois field adder, wherein an output of said Galois field multiplier is further coupled to a second input of said Galois field adder; and said state machine controls respective select lines for each of said multiplexers (figure 9a, 9b, 9c, col. 19, line 12 – col. 20, line 37, Maki et al.).

- As per claim 47, Patel, Stenerson and Maki et al. teach the additional limitations.

Maki et al. teach the decoder circuit further comprising means for determining when an output of said Galois field adder is equal to zero (col. 9, lines 22-30, Maki et al.)

17. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (US 4,504,948) and Stenerson (US 4,597,083) as applied to claim 38 above, and further in view of Wolf (US 6,385,751 B1).

As per claim 41, Patel and Stenerson substantially teach the claimed invention described in claim 38 (as rejected above).

However Patel and Stenerson do not explicitly teach the specific use of the decoder circuit wherein the state machine and the Galois field multiply accumulators are formed in a common application-specific integrated circuit.

Wolf in an analogous art teaches that Reed-Solomon encoders/decoders have been built using chip sets consisting of ASIC (Application Specific Integrated Circuit) processor elements (col. 3, lines 47-49, Wolf). Wolf also teaches that each of the blocks Reed-Solomon control block 403, Galois Field encoder setup block 422, Galois Field decoder setup block 423, encoder 457 and the decoder 458 illustrated in FIG. 4 include a state machine. The state machine flow is illustrated in FIG. 8 (figure 4, 8, col. 10, lines 50-54, Wolf).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel's patent with the teachings of Wolf by including an additional step of using the decoder circuit wherein the state machine and the Galois field multiply accumulators are formed in a common application-specific integrated circuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoder circuit wherein the state machine and the Galois field multiply accumulators are formed in a common application-specific integrated circuit would provide the opportunity to reduce the number of circuit elements and increase the processing speed of Galois field multiply accumulators and the decoder circuit for error correction.

18. Claims 42, 43, 44, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (US 4,504,948) and Stenerson (US 4,597,083) as applied to claim 38 above, and further in view of Shen et al. (US 6,199,188 B1).

As per claim 42, Patel and Stenerson substantially teach the claimed invention described in claim 38 (as rejected above).

However Patel and Stenerson do not explicitly teach the specific use of the decoder circuit wherein: the BCH code is a triple-error correcting code; and there are exactly four of said Galois field multiply accumulators.

Shen et al. in an analogous art teach that the ECC's commonly used with the Galois Fields are Reed Solomon codes or BCH codes. There are essentially four major steps in decoding a corrupted code word of a Reed-Solomon code or a BCH code (col. 1, lines 46-51, Shen et al.). Shen et al. teach that in general, for any degree-three error locator polynomial, the system determines error locations by solving the equation [8], (col. 7, lines 9-11, Shen et al.). Shen et al. also teach a data processing system for determining the roots of a degree-three polynomial that is associated with a data codeword over GF (col. 21, lines 19-21, Shen et al.). Shen et al teach the system wherein the calculating means includes...to produce the cubic root (col. 21, line 52 to col. 22, line 8, Shen et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel's patent with the teachings of Shen et al by including an additional step of using the decoder circuit wherein: the BCH code is a triple-error correcting code; and there are exactly four of said Galois field multiply accumulators.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoder circuit wherein: the BCH code is a triple-error correcting code; and there are exactly four of said Galois field multiply accumulators would provide the opportunity to correct up to 3 errors in the data received using the BCH code and four Galois field multiply accumulators.

- As per claim 43, Patel, Stenerson and Shen et al. teach the additional limitations.

Stenerson teaches the decoder circuit wherein equation (1) is performed using a first one of said Galois field multiply accumulators (col. 18, lines 28-35, Stenerson).

- As per claim 44, Patel, Stenerson and Shen et al. teach the additional limitations.

Stenerson teaches the decoder circuit wherein equation (2) is performed using said first Galois field multiply accumulator and a second one of said Galois field multiply accumulators (col. 18, lines 28-35, Stenerson).

- As per claim 45, Patel, Stenerson and Shen et al. teach the additional limitations.

Stenerson teaches the decoder circuit wherein equation (3) is performed using said first and second Galois field multiply accumulators (col. 18, lines 28-35, Stenerson).

19. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alvarez et al. (US 2002/0165962 A1) in view of Oh et al. (US 5,583,499) and Breiling et al. (Optimum non-iterative turbo-decoding, PIMRC '97, The 8th IEEE International symposium, Sept. 1997, volume 2, pages 714-718).

As per claim 48, Alvarez et al. teach an 0C-192 input/output card comprising: four OC-48 processors; and an OC-192 front-end application-specific integrated circuit (ASIC) connected to said four OC-48 processors, said OC-192 front-end ASIC having means for de-interleaving an OC-192 signal to create four OC-48 signals (figure 17, page 12, paragraphs 192-193, page 30, paragraph 470, Alvarez et al.).

However Alvarez et al. do not explicitly teach the specific use of means for decoding error-correction codes embedded in each of the four OC-48 signals, said decoding means including means for generating an error polynomial associated with a given one of the error-correction codes in no more than 12 clock cycles.

Oh et al. in an analogous art teach that for a t-error correcting Reed-Solomon coder 6t multipliers are needed in calculating the error locator polynomial using the Berlekamp-Massey algorithm, wherein t represents the error correcting capability of the code. The syndrome values are inputted every 2-symbol clock cycles to be used in calculating the error locator polynomial. In other words, it takes two clock cycles in carrying out each iteration (col. 2, lines 19-25, Oh et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Oh et al. by including an additional step of

using means for decoding error-correction codes embedded in each of the four OC-48 signals, said decoding means including means for generating an error polynomial associated with a given one of the error-correction codes in no more than 12 clock cycles.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the time required to determine the locations of the errors.

Alvarez et al. also do not explicitly teach specifically that the decoding means uses a non-iterative algorithm to generate the error polynomial.

However Breiling et al. in an analogous art teach that a new, non-iterative turbo-decoder based on a super-trellis structure is proposed (abstract, Breiling et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Breiling et al. by including an additional step of using the decoding means that uses a non-iterative algorithm to generate the error polynomial.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoding means that uses a non-iterative algorithm to generate the error polynomial would provide the opportunity to reduce Gaussian channel signal-to-noise ratio.

20. Claims 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alvarez et al. (US 2002/0165962 A1), Oh et al. (US 5,583,499) and Breiling et al. (Optimum non-iterative turbo-decoding, PIMRC '97, The 8th IEEE International symposium, Sept. 1997, volume 2, pages 714-718) as applied to claim 48 above, and further in view of Stenerson (US 4,597,083).

As per claim 49, Alvarez et al., Oh et al. and Breiling et al. substantially teach the claimed invention described in claim 48 (as rejected above).

However Alvarez et al., Oh et al. and Breiling et al. do not explicitly teach the specific use of the decoding means that includes a plurality of Galois field multiply accumulators.

Stenerson in an analogous art teaches that the Galois field products from the multiplier 124 (in the form of a PROM programmed as shown in FIGS. 18C and 18D corresponding to multiplying by ff, the coefficient

of the fourth term of the polynomial) are summed by exclusive-Ors 132 with the corresponding outputs of the latches 130 (figure 8, col. 18, lines 28-33, Stenerson).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Stenerson by including an additional step of using the decoding means that includes a plurality of Galois field multiply accumulators.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoding means that includes a plurality of Galois field multiply accumulators would provide the opportunity to generate an error location polynomial and using the error location polynomial determine the location of errors in the code word.

- As per claim 50, Alvarez et al., Oh et al., Breiling et al. and Stenerson teach the additional limitations.

Oh et al. teach that decoding means further includes a state machine for controlling (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

Stenerson teaches the Galois field multiply accumulators (figure 8, col. 18, lines 28-33, Stenerson).

21. Claims 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alvarez et al. (US 2002/0165962 A1), Oh et al. (US 5,583,499), Breiling et al. (Optimum non-iterative turbo-decoding, PIMRC '97, The 8th IEEE International symposium, Sept. 1997, volume 2, pages 714-718) and Stenerson (US 4,597,083) as applied to claim 49 above, and further in view of Shen et al. (US 6,199,188 B1).

As per claim 51, Alvarez et al., Oh et al., Breiling et al. and Stenerson substantially teach the claimed invention described in claim 49 (as rejected above). Stenerson also teaches Galois field multiply accumulators (figure 8, col. 18, lines 28-33, Stenerson).

However Alvarez et al., Oh et al., Breiling et al. and Stenerson do not explicitly teach the specific use of the decoding means to generate an error polynomial for a Bose-chaudhuri-Hbcquenghem (BCH) triple-error correcting code.

Shen et al. in an analogous art teach that there are essentially four major steps in decoding a corrupted code word of a Reed-Solomon code or a BCH code. The system first determines error syndromes that

are based on the results of a manipulation of the ECC symbols. Next, using the error syndromes, the system determines an error locator polynomial, which is a polynomial that has the same degree as the number of errors (col. 1, lines 49-55, Shen et al.). Shen et al. also teach determining three error locations. In general, for any degree-three error locator polynomial, sigma(x), the system determines error locations (col. 7, lines 8-10, Shen et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Shen et al. by including an additional step of using the decoding means to generate an error polynomial for a Bose-chaudhuri-Hbcquenghem (BCH) triple-error correcting code.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoding means to generate an error polynomial for a Bose-chaudhuri-Hbcquenghem (BCH) triple-error correcting code would provide the opportunity to determine error locations using the roots of the error polynomial.

- As per claim 52, Alvarez et al., Oh et al., Breiling et al., Stenerson and Shen et al. teach the additional limitations.

Shen et al. teach that the decoding means includes no more than four of said Galois field multiply accumulators (col. 21, lines 19-21, col. 21, line 52 - col. 22, line 8, Shen et al.).

- As per claim 53, Alvarez et al., Oh et al., Breiling et al., Stenerson and Shen et al. teach the additional limitations.

Stenerson teaches Galois field multiply accumulators (figure 8, col. 18, lines 28-33, Stenerson).

Shen et al. teach that decoding means includes means for computing a plurality of BCH syndromes which are used by said Galois field multiply accumulators to generate the error polynomial (figure 4, col. 1, lines 49-55, col. 12, lines 30-33, Shen et al.).

22. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alvarez et al. (US 2002/0165962 A1), Oh et al. (US 5,583,499) and Breiling et al. (Optimum non-iterative turbo-decoding, PIMRC '97, The 8th IEEE International symposium, Sept. 1997, volume 2, pages 714-718) as applied to claim 48 above, and further in view of Shen et al. (US 6,199,188 B1).

As per claim 54, Alvarez et al., Oh et al. and Breiling et al. substantially teach the claimed invention described in claim 48 (as rejected above).

However Alvarez et al., Oh et al. and Breiling et al. do not explicitly teach the specific use of the decoding means that locates errors within the data signal by applying Chien's algorithm to the error polynomial to search for error location numbers.

Shen et al. in an analogous art teach that in prior systems, the roots of degree-four polynomials are determined by trial and error, or by matrix manipulation or look-up table. The trial and error method is performed by substituting into the polynomial every possible value, i.e., every element of the applicable GF(2.sup.2m) that is associated with a code word location, and for each value evaluating the polynomial. If the polynomial equals zero for a given value, the value is a root. The system continues the trial and error process by substituting a next possible value into the polynomial and determining if that value is a root; and so forth, until either all-possible values have been tried or all four roots are determined. This trial and error process, which in an optimized form is commonly known as a Chien Search, is time consuming. Further, the time is unpredictable, since it varies with the locations of the errors in the code words (col. 2, lines 1-15, Shen et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Shen et al. by including an additional step of using the decoding means that locates errors within the data signal by applying Chien's algorithm to the error polynomial to search for error location numbers.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoding means that locates errors within the data signal by applying Chien's algorithm to the error polynomial to search for error location numbers would provide the opportunity to determine the location of all the errors in the code word by determining all roots of the error locator polynomial.

23. Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (US 6,199,188 B1) as applied to claim 1 above, and further in view of Breiling et al. (Optimum non-iterative

turbo-decoding, PIMRC '97, The 8th IEEE International symposium, Sept. 1997, volume 2, pages 714-718).

As per claim 55, Shen et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Shen et al. does not explicitly teach the specific use of a non-iterative algorithm to generate the error polynomial from the data signal.

However Breiling et al. in an analogous art teach that a new, non-iterative turbo-decoder based on a super-trellis structure is proposed (abstract, Breiling et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shen et al.'s patent with the teachings of Breiling et al. by including an additional step of using a non-iterative algorithm to generate the error polynomial from the data signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a non-iterative algorithm to generate the error polynomial from the data signal would provide the opportunity to reduce Gaussian channel signal-to-noise ratio.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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